VLSI Testing and Security

Set-up of scan based attacks and RT level countermeasures evaluation

Collaboration between
Defacto Technologies (www.defactotech.com)
and
Grenoble INP - LCIS (lcis.grenoble-inp.fr)

Designing secure ICs requires fulfilling many design rules in order to protect access to secret data. However, these security design requirements may be in opposition to test needs and testability improvement techniques that increase both observability and controllability. Nevertheless, secure chip designers cannot neglect the testability of their chip; a high quality production testing is primordial to ensure a good level of security since any faulty devices could induce major security vulnerability.

SoC designers must then apply ad hoc solutions in order to add security features protecting the design and associated data confidentiality. Such techniques are well known by secure IC designers but are not easy to handle for non specialists. Nevertheless, security is becoming an issue for most of the applications and then non security specialist may have to apply such techniques. In this work, we propose to develop a design tool for securing SoC test architecture at RT level which addresses any designers. Most secure DfT techniques are proposed at gate level and then often require major modification late in the design flow, working at RT level reduces the design time and then the cost.

The internship will first aim at developing an RT level method for the evaluation of the design vulnerabilities against test based attacks. This tool will be based on RT level Design for Test tools developed by Defacto. Attacks will be simulated at RT level. Then secure DfT techniques at RT level based on the same tools will be proposed and evaluated.

Required knowledge: VHDL, VLSI design, C

The internship will be based in the LCIS a Grenoble Institute of Technology Research lab located in Valence (connected directly by high speed train to Lyon (30 mins) and (Paris 2h10mins).

Contact and Application by email to:
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